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Optimization of Ultrasonic Scalpel for Neurosurgery

Background

- The Ultrasonic Scalpel for Neurosurgery uses histotripsy to remove unwanted tissue from the brain.
- Histotripsy utilizes high intensity acoustic energy to create cavitation. This cavitation will cause mechanical ablation of unwanted tissue (tumors) in the brain.
- The current iteration has an external high voltage power supply to convert input AC to high voltage DC required for the Ultrasonic Scalpel as well as an external function generator to develop and vary the necessary electrical waveform signals.

Project Scope

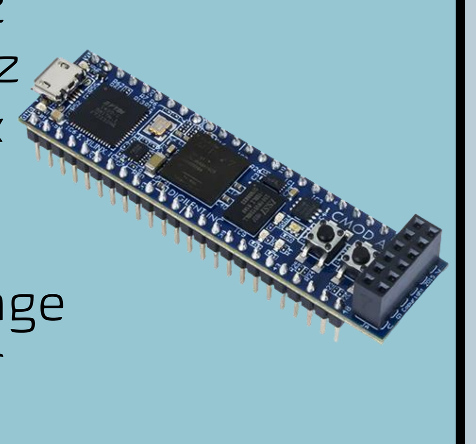
- For this project, the scope is defined as integrating the high voltage power supply, function generator and existing pulser board into a single PCB as follows:
- Integrate HVPS onto pulser PCB
  - Use 15V wall wart as PS
  - Output 0V-200V @ 20-30mA
  - Continuous user selectable output voltage
  - Display current voltage level.
- Integrate function generator onto pulser PCB
  - FPGA programmed as function generator
  - User discrete select output frequencies of 5.5, 6.0, 6.5 MHZ
  - Duty cycle of 50% at 1kHz pulse repetition frequency (PRF).

New Component Highlights

- FS02-12 DC-HVDC Converter provides up 0-200V DC output from adjustable 12V DC control circuit.
- Significant cost and space savings in comparison to bench top HV power supply.

https://www.xppower.com/product/FS-Series

- CMOD A7-15T FPGA 12 MHz clock is upscaled to 250 MHz via onboard 100 MHz VCO & Vivado IP software tool.
- Onboard SRAM means no additional circuitry for storage and load of signal generator program on start-up.

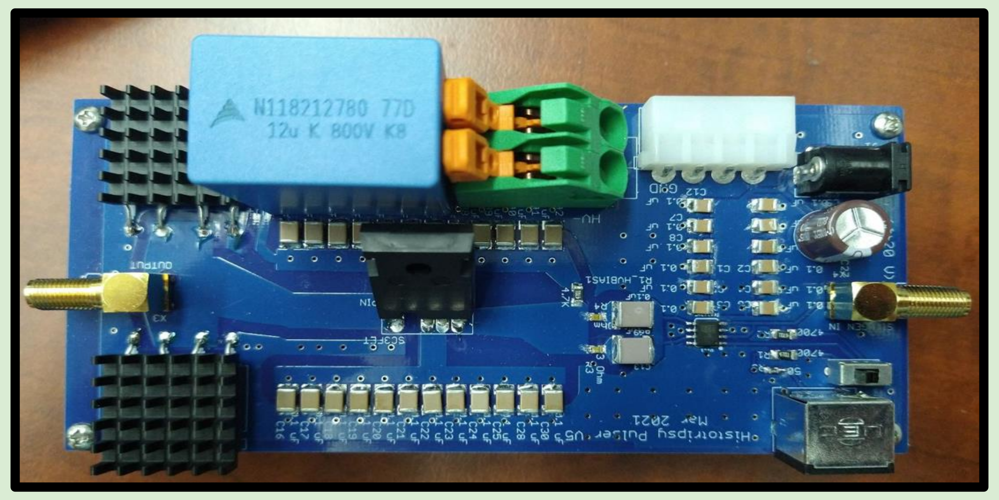


https://digilent.com/reference/programmable-logic/cmod-a7

Design Process

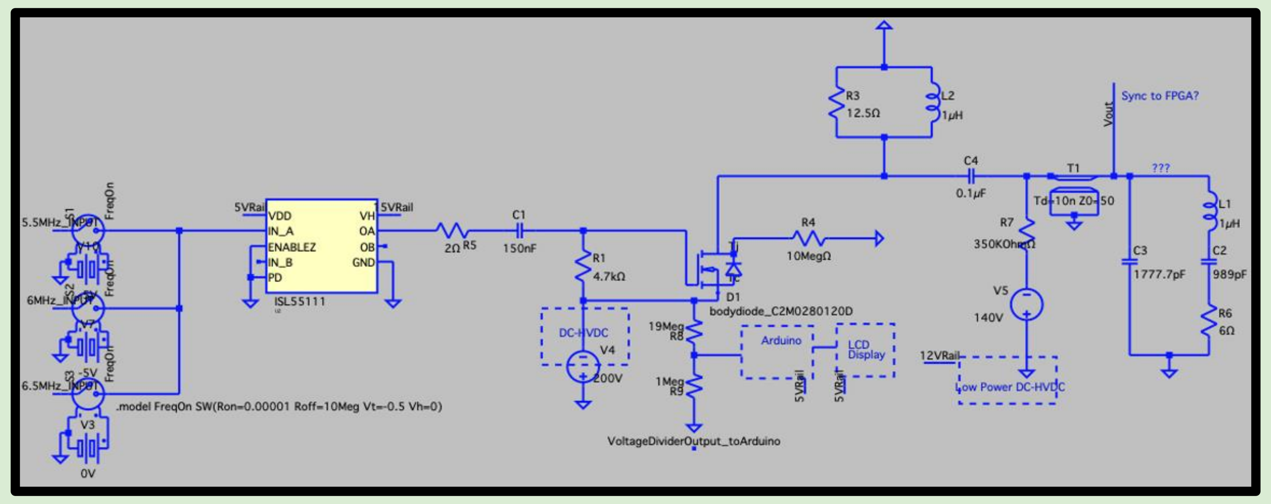
- Main design goals were to achieve same performance output as current iteration of pulser board, eliminate external devices, and significantly reduce deployment cost.
- Development and simulation was devoted to continuing within customer's software design environments for continuity of project.
- Workload was divided between group members to ensure concurrent development of high voltage power supply and FPGA signal generator over project timeline.

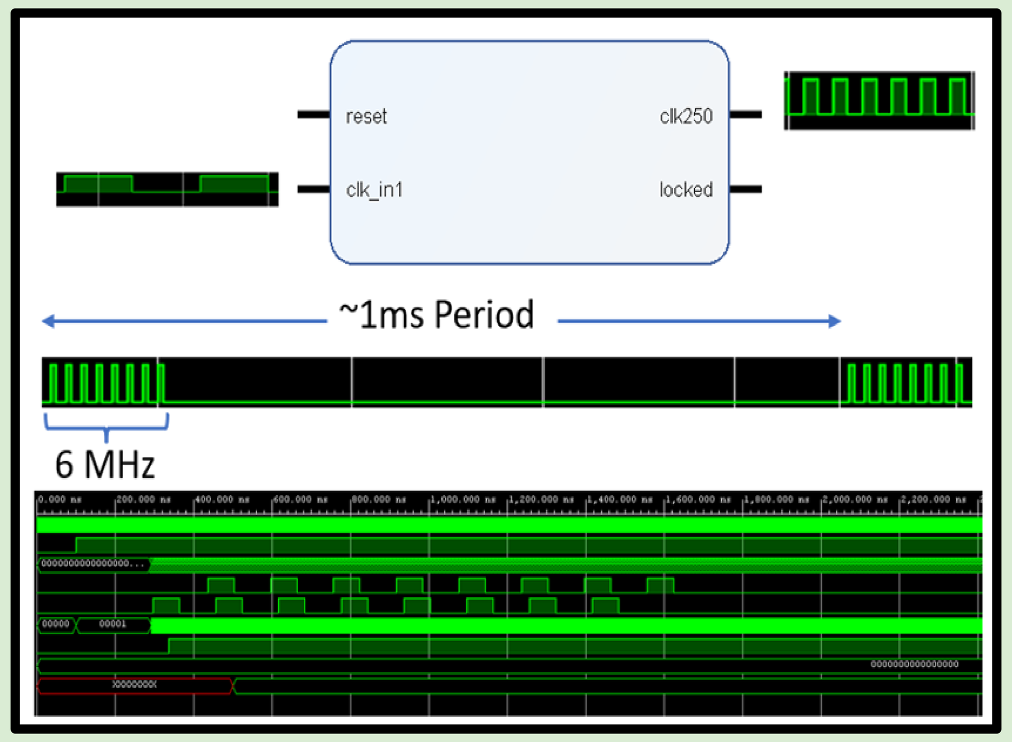
Design Ideas → LTSpice Model & Verilog Code → Software Simulation → Hardware Testing → PCB Design



- Original pulser board includes connections for external HV-PS (green connector top middle) and signal generator (right SMA connector).
- Signal generator transmits desired pulse to gate driver IC. O/P of gate driver IC feeds Silicon Carbide FET (SiCFET) gate pin, providing switching capability for high voltage pulse O/P to transducer.

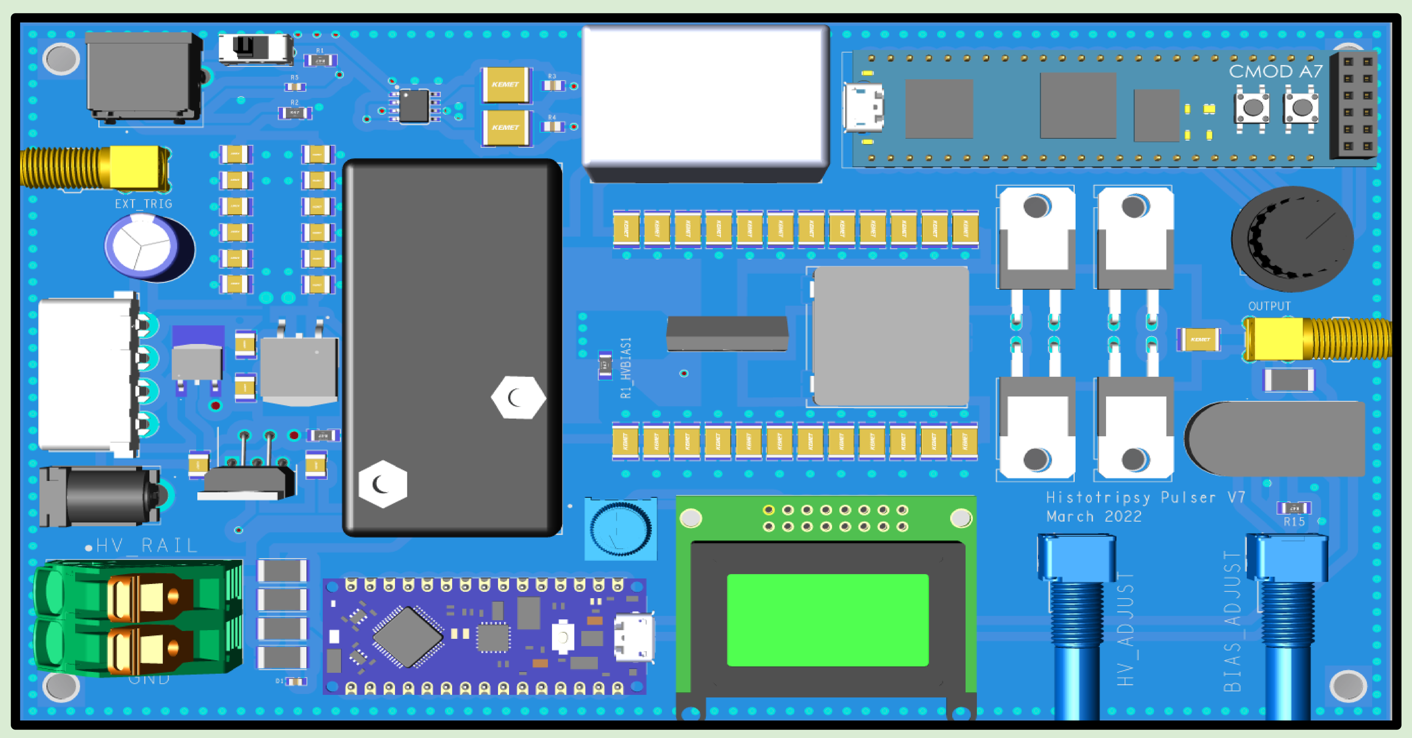
- LTSpice circuit simulates 15V down to 12V and 5V voltage regulation to power DC-DC converters, FPGA, and voltage monitoring components.
- High voltage sources used to simulate DC-HVDC +200V DC source and negative DC-DC voltage bias for output to transducer.





- The Vivado IP tool upscales 12 MHz system clock to 250 MHz signal generator clock.
- Separate registers coded to achieve desired output frequencies of 5.5 – 6.5 MHz (19 bit) and PRF of ~1kHz (1000 bit) by bit-shifting through respective registers on 250 MHz clock pulses.
- Logic coded in Verilog to monitor internal and external trigger signals for pulse activation & freq. select.

- New component footprints created in OrCAD for PCB design.
- LTSpice circuit recreated in OrCAD and PCB designed to combine required original pulser board components and new circuit components.
- PCB sent for manufacture and to be populated for delivery to customer.



Testing & Results

- Sub circuit responsible for controlling the FS02-12 DC-HVDC was created through breadboarding.
  - Driving the HVDC converter includes a linear voltage regulator and a potentiometer to allow for an adjustable output.
  - Results were in line with the previous iteration of the board using the dedicated power supply.
- The CMOD A7-15T FPGA was connected to the preceding revision of the pulser board to generate an output.
  - Test results were comparable to using a dedicated external function generator.
- Successful results lead to PCB manufacturing.

Conclusion & Additional Development

- The final design achieves the required output and removes the external devices, incorporating all components into a 6" x 8" PCB.
- All internal signals needed come from a 120Vac to 15V DC wall wart for ease of use and versatility for collaborators.
- HVDC supply pins have been added to allow for the board to alternatively be powered by external PS. This will be used for future testing, and to further technological studies.
- The Digilent CMOD A7-15T has recently been discontinued by the manufacturer. The recommended replacement is the CMOD A7-35T which has the same Artix-7 FPGA and pin layout for easy integration into future designs.

References

Sukovich, J. R., Cain, C. A., Pandey, A. S., Chaudhary, N., Camelo-Piragua, S., Allen, S. P., . . . Xu, Z. (2019). In vivo Histotripsy Brain treatment. *Journal of Neurosurgery, 131*(4), 1331-1338. doi:10.3171/2018.4.jns172652