DALHOUSIE UNIVERSITY
FACULTY OF ENGINEERING

Team #4 Members: Nathaniel Coolen-Jewers, Tyler Grandy, Will Haas & Moyo Oni
External (Client) Supervisors: Eric Mullaley & Ian MacKay (P.Eng)
Internal Supervisor: Dr. Yuan Ma

MOOG FOCAL™

Department of Electrical and Computer Engineering

Automated Multiplexer Test System

Project Background

Quality testing and verification is an important step in every engineering design process, it can consume time and money quickly. Therefore, under the supervision of Dalhousie University and Moog Focal Industries, the goal of this team project is to develop automated test system in the form of separate Verilog Modules for each Input/Output function of the 924 Multiplexer Board. Verilog is a hardware description language; in this project it will be used to control the Xilinx Kintex-7 Field Programmable Gate Array (FPGA). Essentially the system will consist of pressing one button to activate the program and initiate the multiplexer to self-test and verify each Input/Output function.

The focus of this Capstone Team will be to develop the Serial Data and Ethernet Data testing modules interlinked with the Testing Interface.

Design Process

Phase 1: Verilog Research/Training
- Training and research into the Verilog language. (New to team)
- Creation of a stopwatch module as a practice exercise/challenge

Phase 2: Serial Test
- Determine test requirements and development process
- Development of serial stimulus module
- Development of serial verification module
- User interface/GUI creation
- Implementation of serial test into UI

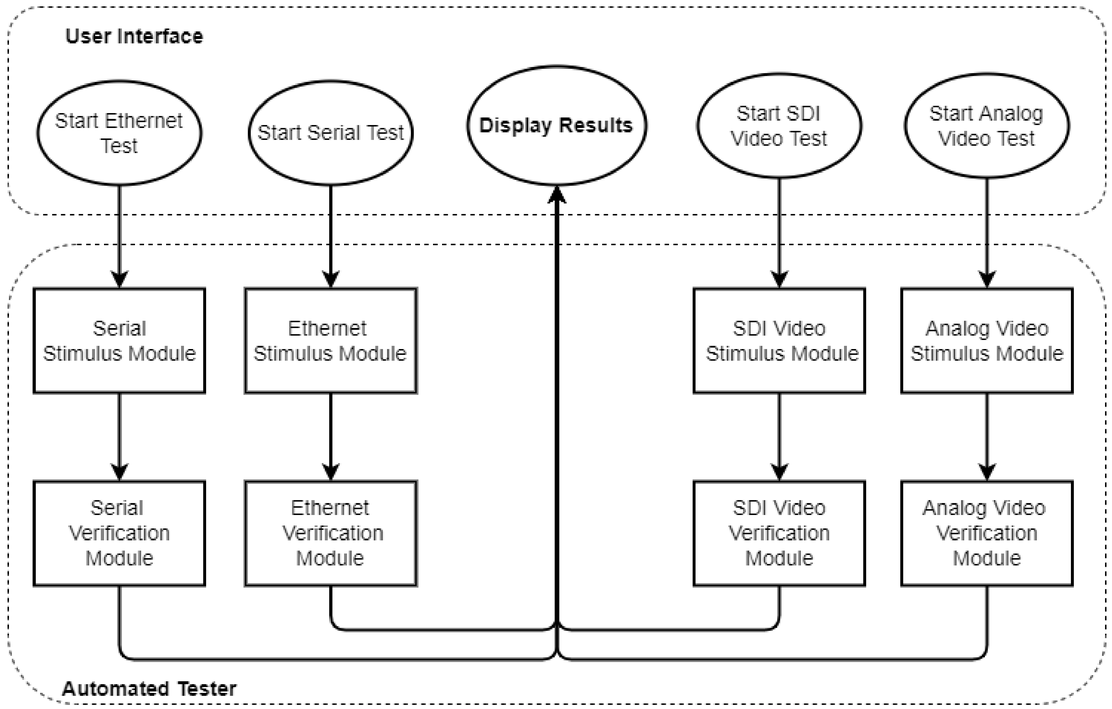
Phase 3: Ethernet Test
- Development of Ethernet stimulus module
- Development of Ethernet Verification module
- Integration of Ethernet test into UI

Phase 4: Analog/SDI Video Test
- If the team has successfully accomplished serial and ethernet test creation (Main focus), team may move into phase 4 and choose to develop Analog and/or SDI video tests

Design Details

The project proposal from the client specifies that automated testing systems for at least two of the boards four data formats (Serial, Ethernet, Analog Video, SDI Video) will be developed, as well as a user interface/GUI. These tests are achievable by wiring the I/O ports with a loop back mechanism, this can be done with a connector that shorts the transmission (TX) and receiver (RX) pins to each other, allowing any given port to send data to itself. From these requirements the team created the system architecture consisting of a generation and verification module for each data type as seen below:

System Architecture



In the system architecture, each of the four tests are represented by a stimulus module and a verification module, which integrates back into the user interface. The general design of these modules can be seen below:

General Test Design

Stimulus (Transmitter)
- Start/Stop Control
- Transmission Rate Control
- Transmission Duration Control
- Error Detection Mechanism (Parity bit, checksum, etc)
- Data Pattern/Signal

Verification (Receiver)
- Receive Transmission Rate
- Receive Transmission Duration
- Receive Data Accurately
- Determine Number of Errors
- Store Results in Memory

User interface Implementation
- Input Parameters (Start, Stop, Test Type, etc.)
- Read test results from memory
- Display formatted test results

Team Recommendations

- Project team could benefit from taking IC Design and Fabrication as a technical elective as it covers FPGA's
- Time to learn Verilog should be allocated with potential for extensions to aid understanding and competence
- Required modules are segmented into smaller tasks aiding the allocation of work and monitoring of progress
- Basic comprehension of system architecture is necessary for the understanding of the overall project especially when implementing multiple modules

Conclusion

Moog Focal spends a considerable amount of resources on the testing and verification stage of the design process to ensure the consumer receives a high quality product. The project teams goal is to design and code Verilog modules to utilize existing hardware to test and verify the Input/Outputs on the device help reduce the cost of this stage for the companies multiplexer product line. The team has spent the beginning of the term learning the syntax and basics of Verilog coding, therefore, the team expects to work a small amount in the summer term to gain progress on the current Serial Data module. The team would like to have the Serial Data and Ethernet Data modules as well as the UI coded and implemented into the Automated Test System by the end of the Fall academic term in December of 2022.

References

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