DALHOUSIE UNIVERSITY
FACULTY OF ENGINEERING

Improved Noise Shaping Digital Delta-Sigma Modulation

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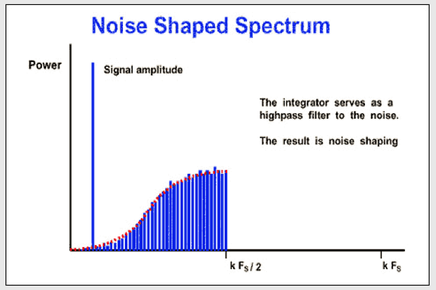
Client: Dr. El-Sankary, Colin Ross

Scope of Work

Design and recommend different delta-sigma modulator architecture, as well as design a testing flow for future delta-sigma modulator implementations.

Background

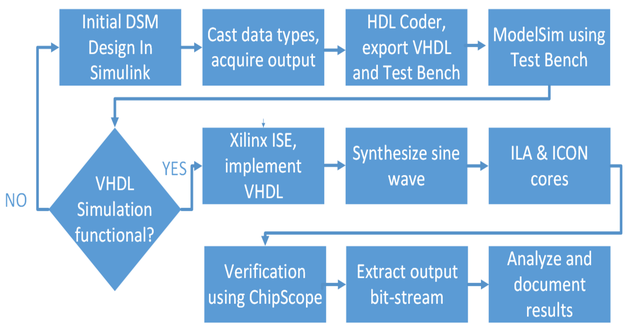
Noise Shaping Theory



Why 1-bit Delta-Sigma architecture?

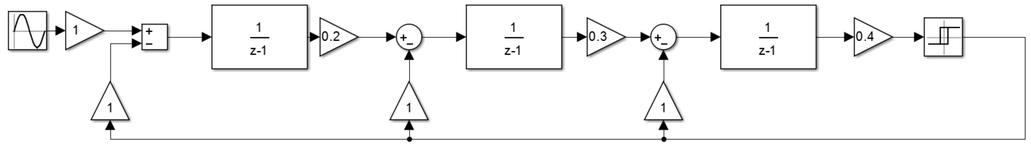
- Less power
- Less area
- Intrinsically linear
- Voltage is too low for multiple quantization levels
- Compensated with high order architecture and high sampling rate

Design Process

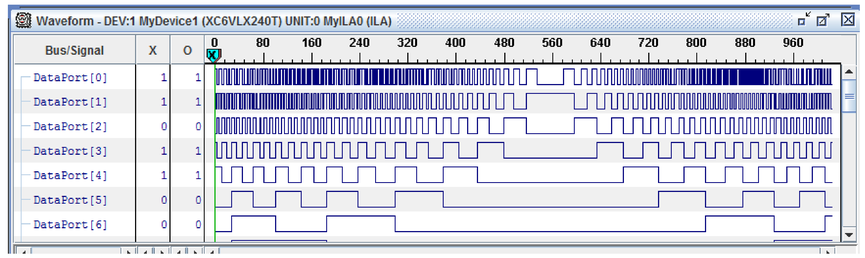


Details of Final Design

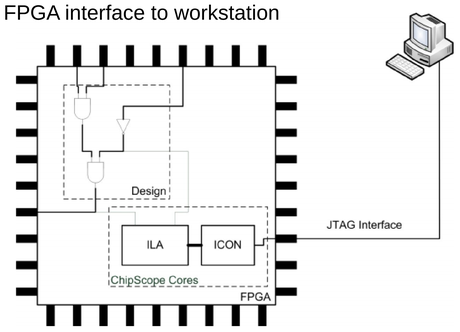
Third order DSM SIMULINK model



Synthesized sine wave output

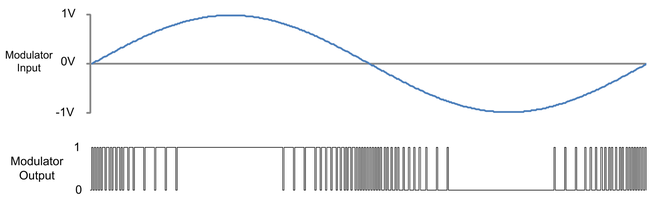


FPGA interface to workstation



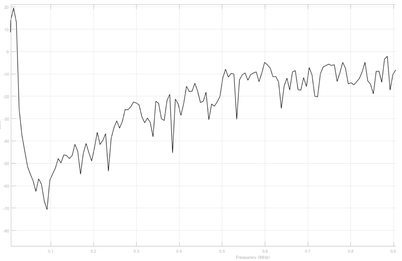
Implementation utilized in FPGA design which allows real time communication between the FPGA and a computer using the JTAG interface. The ICON core establishes a connection to the computer, while the ILA core communicates signal data to the ICON core.

Third order ChipScope bitstream. Testing in MATLAB showed that there was no noise shaping present in this output. Troubleshooting will be needed to fix this irregular output.



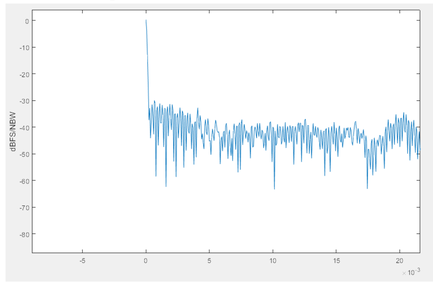
Typical bitstream showing how the amplitude and frequency information is present even in a 1-bit signal

MATLAB simulation output



Expected output from third order Simulink model. Noise shaping is clearly visible.

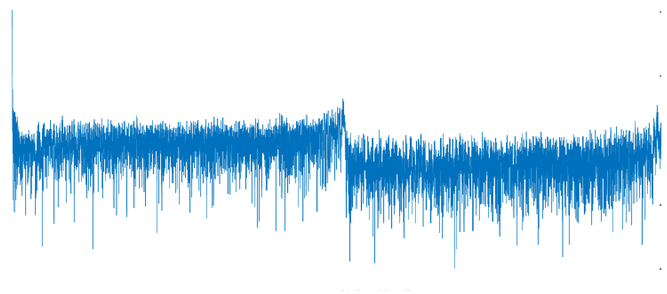
FPGA design results



Achieved output. No noise shaping present, more investigation to be performed into the lack of performance.

Unexpected Output

Unexpected jittering happened each period of the output signal. This manifested as an unwanted frequency component as seen in the spectrum below.



Conclusion and Recommendations

A testing flow with accompanying user manual was developed to test and implement various delta-sigma architectures. Testing will have to continue to appropriately determine suitable architecture.

References

- "Demystifying Delta-Sigma ADCs." *Demystifying Delta-Sigma ADCs - Tutorial - Maxim*. Maxim Integrated, n.d. Web. 19 Mar. 2017.
- *COE 758 – Xilinx ISE 13.4 Tutorial 2* (n.d.): n. pag. Ryerson. Web. <http://www.ee.ryerson.ca/~lkirisch/ele758/handouts/Tutorial2_ChipScope_Part_1.pdf>.